ABSTRACT OF THE DISCLOSURE

A circuit for glitch-free changing of clock having different phases. The circuit comprises a phase detector for receiving a data stream and a system clock, and generating a phase-up signal and a phase-down signal; a flag signal generator for receiving the phase-up signal and the phase-down signal, and then generating M flag signals, wherein the select signal corresponding to the enabled flag signal is enabled; an output stage for receiving the M select signals and the M clocks, and then outputting the system clock.